

AMENDMENTS TO THE CLAIMS

1. (Original) A control circuit for use in an apparatus, comprising:

a plurality of sensor boards connected in cascade so that said plurality of sensor boards define a signal path that runs through the plurality of sensor boards, each of said plurality of sensor boards being connected to a corresponding sensor and providing a sensor output of the corresponding sensor to the signal path; and

a main control board connected to a first one of said plurality of sensor boards and to a final one of the plurality of sensor boards;

wherein when said main control board provides a first signal to the first one of the plurality of sensor boards, each of said plurality of sensor boards provides the sensor output onto the signal path at a predetermined timing and said main control board receives the sensor output at the predetermined timing, the sensor output signal being output in an order in which the plurality of sensors are connected in cascade.

2. (Original) The control circuit according to Claim 1, wherein when a preceding one of two consecutive sensor boards of said plurality of sensor boards is active, the preceding one provides a second signal to a following one of the two consecutive sensor boards;

wherein when the preceding one does not provide the second signal to the following one, the following one provides a corresponding sensor output onto the signal path.

3. (Currently amended) The control circuit according to Claim [[1]] 2, wherein when the preceding one provides the second signal to the following one, said main control board receives the sensor output of the preceding one.

4. (Original) The control circuit according to Claim 1, wherein the sensor is a digital sensor.

5. (Original) The control circuit according to Claim 1, further comprising an analog-to-digital converter;

wherein the sensor is an analog sensor that generates an analog sensor output and said analog-to-digital converter converts the analog sensor output into a digital signal.

6. (Currently amended) The control circuit according to Claim 1, wherein each of said plurality of sensor boards includes the sensor on one side thereof and a bare 1C chip on the other side, the bare 1C chip incorporating all of the required circuits.

7. (Currently amended) The control circuit according to Claim 1, wherein each of said plurality of sensor boards includes an input that ~~receive~~ receives an incoming

signal and a terminator connected to the input, the terminator setting an input impedance of the input.

8. (Currently amended) The control circuit according to Claim 1, further comprising a sensor check circuit;

wherein said main control board provides the first signal to the first one of said plurality of sensor boards to activate a cycle of receiving a train of sensor outputs from the final one of said plurality of sensor boards;

wherein said sensor check circuit determines whether the train of sensor outputs of a preceding one of the two consecutive cycles is different from the train of sensor outputs of a following one of the two consecutive cycles;

wherein if the train of sensor outputs of the following one of the two consecutive cycles is different from the train of sensor outputs of the preceding one of the two consecutive cycles, said sensor check circuit provides a third signal to said main control board so that said main control board performs a predetermined control operation.